Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A system having an insertion sorter circuit for determining a predetermined number N of most significant values of a set of random values comprising:

a plurality of N series-connected sorter elements SE_i, for each integer i from 1 to N, for sequentially processing the set of random values;

each sorter element SE_i sequentially receiving the random values from a respective one of N parallel inputs and including:

a register R_i for storing a most significant value; and

a two element comparator C_i for comparing the stored R_i value to a received value of the set of random values; and

each sorter element SE_i for $i>1$, also including:

a multiplexer M_i for selecting between the received value and a register stored value and loading the selected value into the register R_i when the received value is greater than the stored R_i value;

sorter element SE_1 configured to load the received value into register R_1 when the received value is greater than the value stored in R_1; and

said sorter elements SE_1 to SE_N connected in series such that, for each $i>1$, the register stored value of the multiplexer M_i is output from the register R_{i-1} when the comparator C_{i-1} determines that the received value is greater than the R_{i-1} stored value, whereby the registers R_1 to R_N store N most significant values in a descending order after sequentially processing the set of random values.

2. (previously presented) The system of claim 1 further comprising:

an adder for summing the random values which are not stored as most significant values after sequentially processing the set of random values; and

a register for storing the sum of the random values not stored as most significant values.

3. (previously presented) The system of claim 2 which further comprises a circuit for processing received communication data to produce a set of random values representing midamble tap sequence values of a communication signal which are provided to said sorter circuit for processing whereby the N most significant values after sequentially processing the set of random values represent N channel response values of the communication signal, and the sum of the random values, which does not include the N most significant values after sequentially processing the set of random values, represents noise of the communication signal.

4. (currently amended) The system of claim 2 where the sorter elements SE_1 to SE_N and the adder operate in parallel to simultaneously process one random value during each processing cycle such that the number of processing cycles needed for sorting and summation is equal to the number of values in the set of random values that are sorted, whereby clock speed of the sorter circuit is unaffected by the number N of sorter elements.

5. (previously presented) A system which processes received communication data where a set of random values represents midamble tap sequence values of a communication signal, N most significant values of the set of random values represent N channel response values of the communication signal, and the sum of the random values

which does not include the N most significant values of the set of random values represents noise of the communication signal comprising:

a plurality of N series-connected sorter elements SE_i, for each integer i from 1 to N, for sequentially processing the set of values;

each sorter element SE_i sequentially receiving the random values from a respective one of N parallel inputs and including:

a register R_i for storing a most significant value; and

a two element comparator C_i for comparing the stored R_i value to a received value of the set of random values; and

each sorter element SE_i for $i>1$, also including:

a multiplexer M_i for selecting between the received value and a register stored value and loading the selected value into the register R_i when the received value is greater than the stored R_i value;

sorter element SE_1 configured to load the received value into register R_1 when the received value is greater than the value stored in R_1; and

said sorter elements SE_1 to SE_N connected in series such that, for each $i>1$, the register stored value of the multiplexer M_i is received from the register R_{i-1} when the comparator C_{i-1} determines that the received value is greater than the R_{i-1} stored value whereby the registers R_1 to R_N store N most significant values in a descending order after sequentially processing the set of random values; and

an adder circuit for summing the random values which are not stored as most significant values after sequentially processing the set of random value, the adder circuit also sequentially receiving each of the random values simultaneously with said sorting elements and a register stored value from the register R_N when the comparator C_N determines that a received value is greater than the R_N stored value including:

a register R_S for storing the sum of the random values not stored as most significant values; and

an adder which sums the value stored in the register R_S with the lesser of the received random value and the register stored value of the register R_N and stores the summed value in register R_S.

6. (previously presented) The system of claim 5 where the sorter elements SE_1 to SE_N and the adder circuit operate in parallel to simultaneously process one random value during each processing cycle such that the number of processing cycles needed for sorting and summation is equal to the number of values in the series of random values that are sorted, whereby clock speed of the sorter circuit is unaffected by the number N of sorter elements.

7-9. (canceled)

10. (currently amended) A method for processing received communication data where a set of random values represent midamble tap sequence values of a communication signal, N most significant values of the series of random values represent N channel response values of the communication signal, and a sum of the random values that do not include the N most significant values of the set of random values, the sum representing noise of the communication signal, the method for determining the N channel response values and noise of the communication signal comprising:

sequentially processing the series of random values using an adder circuit having a register R_S initialized with a zero value and a series of sorter elements SE_i, for each integer i from 1 to N, each sorter element SE_i having a register R_i initialized with a zero value and a comparator C_i;

sequentially receiving the random values from one of N+1 respective parallel inputs by each sorter element SE_i and the adder circuit;

for each received random value, the first sorter element SE_1:

compares the stored R_1 value to the received value; and

stores the selected value into the register R_1 when the received value is greater than the existing stored R_1 value;

for each received random value, each sorter element SE_i, for $i > 1$:

compares the stored R_i value to the received value; and

stores a new value into the register R_i when the random value is greater than the existing stored R_i value, and the new value being the random value, except when sorter element SE_{i-1} determines that the received value is greater than the R_{i-1} stored value, in which case the new value stored in register R_i is the register R_{i-1} value, whereby N most significant values are stored in a descending order in registers R_1 to R_N after processing all values of the set of random values, the N most significant values representative of N channel response values of the communication signal; and

for each received random value, the adder circuit:

sums the value stored in the register R_S with the lesser of the received random value and the R_N stored value; and

stores the summed value in register R_S whereby the sum of the values of the random value series which are not stored as most significant values is stored in register R_S after sequential processing of the random value series is completed, the sum representative of the noise of the communication signal.

11. (currently amended) The method of claim 10 where the sorter elements SE_1 to SE_N and the adder circuit operate in parallel to simultaneously process one random value during each processing cycle such that the number of processing cycles needed for sorting and summation is equal to the number of values in the series of random values that are sorted, whereby clock speed of the sorter circuit is unaffected by the number N of sorter elements.

12. (canceled)